



07/21/97

1260-101

A

Attorney's Docket No. 73305.P066PatentASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231SIR: Transmitted herewith for filing is the **nonprovisional patent application** ofInventor(s): Donald Victor Perino, John Brady Dillon and James Anthony GasbarroFor: MULTI-POSITION CONNECTOR WITH INTEGRAL TRANSMISSION LINE BUS

(Title)

Enclosed are:

- ☒ Eleven (11) sheet(s) of Drawings.
 _____ An Assignment of the Invention to _____
 _____ Assignment Cover Sheet Form PTO-1595.
☒ A Declaration and Power of Attorney (signed/ ☒ unsigned).
 _____ A Verified Statement to establish Small Entity Status under 37 C.F.R. §§ 1.9 and 1.27.

The Filing Fee has been calculated as shown below:

	(Col. 1)		(Col. 2)	
For:	No. Filed		No. Extra	
Basic Fee:				
Total Claims:	35	- 20	*	15
Indep. Claims:	5	- 3	*	2
<input type="checkbox"/> Multiple Dependent Claim(s) Presented				

* If the difference is less than zero,
enter "0" in Col. 2.

SMALL ENTITY	
Rate	Fee
	\$ 385
x 11	\$
x 40	\$
+ 130	\$
TOTAL	\$

OTHER THAN A SMALL ENTITY	
Rate	Fee
	\$ 770
x 22	\$ 330
x 80	\$ 160
+ 260	\$
TOTAL	\$ 1,260

- ☒ A check for \$ 1,260.00 for the filing fee is enclosed.
 _____ A check for \$ _____ for recordation of the Assignment is enclosed.

"Express Mail" mailing label number: EM501832065USDate of Deposit: July 21, 1997

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Patricia A. Balero

(Typed or printed name of person mailing paper or fee)

Patricia A. Balero
(Signature of person mailing paper or fee)07/21/97

(Date signed)

X The Commissioner of Patents and Trademarks is hereby authorized to charge payment of the following fees associated with this communication, or credit any overpayment, to our Deposit Account No. 02-2666. **A duplicate copy of this sheet is enclosed.**

 X Any additional filing fees required under 37 C.F.R. § 1.16.

 X Any patent application processing fees under 37 C.F.R. § 1.17.

 X The Commissioner of Patents and Trademarks is hereby authorized to charge payment of the following fees during the pendency of this application, or credit any overpayment, to our Deposit Account No. 02-2666. **A duplicate copy of this sheet is enclosed.**

 X Any processing fees under 37 C.F.R. § 1.17, including any extension fees.

 X Any filing fees under 37 C.F.R. § 1.16 for presentation of extra claims.

 X Send all correspondence to the undersigned at BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard, Seventh Floor, Los Angeles, California 90025, and direct all telephone calls to the undersigned at (408) 720-8598.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: 7 - 21, 1997

By RBCA
Roland B. Cortes

Reg. No.: 39.152

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8598

Attorney's Docket No. 73305.P066

Patent

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

SIR: Transmitted herewith for filing is the **nonprovisional patent application** of

Inventor(s): Donald Victor Perino, John Brady Dillon and James Anthony Gasbarro

For: MULTI-POSITION CONNECTOR WITH INTEGRAL TRANSMISSION LINE BUS

(Title)

Enclosed are:

- X Eleven (11) sheet(s) of Drawings.
An Assignment of the invention to _____
Assignment Cover Sheet Form PTO-1595.
X A Declaration and Power of Attorney (signed/ X unsigned).
A Verified Statement to establish Small Entity Status under 37 C.F.R. §§ 1.9 and 1.27.

The Filing Fee has been calculated as shown below:

(Col. 1)			(Col. 2)	
For:	No. Filed		No. Extra	
Basic Fee:				
Total Claims:	35	- 20	*	15
Indep. Claims:	5	- 3	*	2
<input type="checkbox"/>	Multiple Dependent Claim(s) Presented			

* If the difference is less than zero,
enter "0" in Col. 2.

SMALL ENTITY	
Rate	Fee
	\$ 385
x 11	\$
x 40	\$
+ 13 0	\$
TOTAL	\$

OTHER THAN A SMALL ENTITY	
Rate	Fee
	\$ 770
x 22	\$ 330
x 80	\$ 160
+ 260	\$
TOTAL	\$ 1,260

- X A check for \$ 1,260.00 for the filing fee is enclosed.
A check for \$ _____ for recordation of the Assignment is enclosed.

"Express Mail" mailing label number: EM501832065US

Date of Deposit: July 21, 1997

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Patricia A. Balero

(Typed or printed name of person mailing paper or fee)

Patricia A. Balero

(Signature of person mailing paper or fee)

07/21/97

(Date signed)

X The Commissioner of Patents and Trademarks is hereby authorized to charge payment of the following fees associated with this communication, or credit any overpayment, to our Deposit Account No. 02-2666. **A duplicate copy of this sheet is enclosed.**

 X Any additional filing fees required under 37 C.F.R. § 1.16.

 X Any patent application processing fees under 37 C.F.R. § 1.17.

 X The Commissioner of Patents and Trademarks is hereby authorized to charge payment of the following fees during the pendency of this application, or credit any overpayment, to our Deposit Account No. 02-2666. **A duplicate copy of this sheet is enclosed.**

 X Any processing fees under 37 C.F.R. § 1.17, including any extension fees.

 X Any filing fees under 37 C.F.R. § 1.16 for presentation of extra claims.

 X Send all correspondence to the undersigned at BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard, Seventh Floor, Los Angeles, California 90025, and direct all telephone calls to the undersigned at (408) 720-8598.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: 7-21, 1997

By RBCA
Roland B. Cortes

Reg. No.: 39,152

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8598

APPLICATION FOR UNITED STATES LETTERS PATENT

**MULTI-POSITION CONNECTOR WITH INTEGRAL TRANSMISSION
LINE BUS**

Inventors:

DONALD VICTOR PERINO
JOHN BRADLY DILLON
JAMES ANTHONY GASBARRO

Prepared by:

Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8598

Attorney's Docket No. 073305.P066

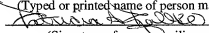
"Express Mail" mailing label number EM501832065US

Date of Deposit July 21, 1997

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee is addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Patricia A. Balero

(Typed or printed name of person mailing paper or fee)


(Signature of person mailing paper or fee)

08607768-072197

MULTI-POSITION CONNECTOR WITH INTEGRAL TRANSMISSION LINE BUS

FIELD OF THE INVENTION

- The present invention relates to electrical interconnects and, in particular,
- 5 connectors for use in high speed electrical interfaces.

BACKGROUND

- In general, electrical connectors consist of two components, a receptacle and a plug. The receptacle is the compliant part of the connector. That is, the receptacle is fashioned in such a way that it provides compliance (or "springiness"), either through the use of a
- 10 springy metal such as a Beryllium-Copper (Be-Cu) alloy or some other means. The plug then forms the non-compliant part of the connector.

- Connectors are used in a variety of applications where electrical coupling between components, e.g., integrated circuits, circuit boards, etc., is desired. However, connectors for high speed interfaces are required to present controlled impedance interconnections.
- 15 The interface between a Rambus DRAM (RDRAM®) and a Rambus Channel is an example of a high speed interface that requires a connector having particular electrical and physical characteristics.

- Since the early 1970s, the essential characteristics of a DRAM interface have remained as a separate data bus and a multiplexed address bus. However, a recent
- 20 architecture pioneered by Rambus, Inc. provides a new, high bandwidth DRAM interface. Originally, the Rambus Channel, the heart of the new DRAM interface, comprised a byte wide, 500 or 533 Mbytes/sec. bi-directional bus connecting a memory controller with a collection of RDRAMs®. Among the many innovative features of the Rambus Channel and of the RDRAM® is the use of vertically or horizontally mounted RDRAMs® and a
- 25 physically constrained, bi-directional bus using terminated surface-trace transmission lines on a circuit board. The physical and electrical properties of both the RDRAMs® and bus on which they are placed are rigidly defined because high frequency operation relies on the

careful physical design of both the printed circuit board and the high speed components. Originally, RDRAMs® were specified to include a 32-pin package, either a surface horizontal package (SHP) or a surface vertical package (SVP).

Electrical connectors of the past have generally been unsuitable for use in high speed bus applications such as may be found with the Rambus Channel. For example, as shown in Figure 1, electrical connectors of the past have employed compliant contact elements 2 to receive semiconductor devices and/or circuit boards to provide electrical coupling to a circuit on a substrate 4 (e.g., a motherboard). The electrical connectors may be contained within housings 6 adapted to receive the semiconductor device or circuit board and are electrically coupled to circuit elements on the motherboard through a solder connection 8. Such a connector thus requires a number of surface mount contacts (e.g., solder contacts 8) between the contact elements 2 and the substrate 4.

Such a connector is not suitable for use in a high speed electrical bus because the contact elements 2 are individually soldered to circuit elements (e.g., electrical traces) on the substrate 4, and because the resulting solder joints 8 are generally not accessible for inspection and repair. High speed bus design dictates that the electrical signal path from device to device be kept at a minimum. Further, electrical contacts on each device should be concentrated into a small area. Together, these requirements lead to a high density area array of separable contacts, whose corresponding solder joints are made inaccessible due to interference from adjacent contacts and/or the contact housing. Except for special "ball grid array" soldering techniques, surface mount solder joints are generally required to be accessible for inspection and repair. Because connectors such as that illustrated in Figure 1 are incapable of meeting these requirements, they are unsuitable for use in high speed bus applications.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide means for electrically coupling a number of substantially similar electrical devices in a substantially bus-like arrangement.

It is a further object of the present invention to provide an electrical connector for use in high speed applications.

A socket is described. The socket may include a first conductor having two or more contact regions and a second conductor arranged substantially parallel to the first conductor and having two or more contact regions. The first and second conductors are spaced relative to one another so as to provide a predetermined electrical impedance. A dielectric spacer may be disposed between the first and second conductors to provide the spacing. Contact regions of the first and second conductors may provide compliant coupling regions for the socket. The first conductor may be further adapted to be coupled to a substrate through only two electrical contact elements over its length, regardless of the number of contact regions of the first conductor. In addition, the second conductor may be further adapted to be coupled to the substrate through a number of electrical contact elements disposed along its length, the number of contact elements being independent of the number of contact regions of the second conductor.

Further described is an electrical connector that includes a socket and a number of conductors disposed therein. The conductors are arranged to carry electrical signals as transmission lines, and are further arranged into a first group of conductors, each adapted to be coupled to a substrate at only two electrical contact elements, and a second group of conductors each adapted to be coupled to the substrate at a plurality of electrical contact elements. The conductors may each include compliant contact regions, each arranged such that the contact regions of a first of the conductors are positioned within the socket so as to contact a lead disposed on a first side of a circuit element and the contact regions of a second of the conductors are positioned within the socket so as to contact a lead disposed

on a second side of the circuit element. A dielectric spacer may be disposed between the first and second conductors.

Also described is a circuit board that includes a compliant electrical connector having a plurality of conductors arranged into a first group of conductors each adapted to be coupled to a substrate at only two electrical contact elements and a second group of conductors each adapted to be coupled to the substrate at a plurality of electrical contact elements. The circuit board further includes an electrical channel, which may include a number of traces, coupled to the connector. Each of the electrical conductors may further include two or more contact regions, the number of contact regions of each conductor being independent of the number of electrical contact elements of a respective conductor.

In addition, a connector that includes a first electrical signal path configured to provide a bus-like interconnection between similar electrical couplings of two or more electrical components, the bus-like interconnection adapted to be isolated from a circuit board except for two electrical contact elements disposed near opposite ends of said first electrical signal path; the connector also including a ground signal path, is described. The ground signal path may be configured as a second electrical signal path arranged to provide a bus-like interconnection between similar electrical couplings of said two or more electrical components. Further, the ground signal path may be adapted to be electrically coupled to a ground plane of the circuit board at a plurality of points along said bus-like interconnection. The first electrical signal path generally includes an electrical conductor having compliant contact regions, which may include elastomer-backed metal regions or may be made of a Beryllium-Copper (Be-Cu) alloy.

Additionally described is a socket that includes a conductive signal bar having two or more contact regions, each adapted to couple to a contact region on a respective electrical device, the signal bar further adapted to be electrically coupled to a circuit board through only two electrical contact elements regardless of the number of contact regions of said signal bar. The socket also includes a conductive ground bar arranged substantially parallel

- to said signal bar and having two or more contact regions, each adapted to couple to a contact region on said respective electrical devices, and further being adapted to be electrically coupled to a conductive reference region of the circuit board at a number of electrical contact elements, the number of electrical contact elements being independent of
- 5 the number of contact regions of the ground bar.

00097788.072197

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the Figures of the accompanying drawings, in which:

Figure 1 illustrates a conventional electrical connector requiring an independent
5 surface mount contact;

Figure 2 illustrates a printed circuit board with a socket configured in accordance with one embodiment of the present invention;

Figure 3A illustrates a cross-sectional view of the printed circuit board shown in Figure 1 and includes features of the socket shown in Figure 1 according to one
10 embodiment of the present invention;

Figure 3B illustrates a cross-sectional view of a bus conductor adapted to carry a ground signal in accordance with an embodiment of the present invention;

Figure 4 illustrates one means of providing a desired spacing for electrical conductors within a socket according to one embodiment of the present invention;

Figure 5 illustrates an electrical channel according to a further embodiment of the
15 present invention;

Figure 6A illustrates an alternative conductor with contact regions for use according to a further embodiment of the present invention;

Figure 6B illustrates the conductor of Figure 5A with contact regions bent to
20 provide desired electrical characteristics in accordance with a further embodiment of the present invention;

Figure 7 illustrates one embodiment of a Daughter card for use with a socket configured according to one embodiment of the present invention;

Figure 8 illustrates a pair of conductors with contact regions arranged in accordance with an alternative embodiment invention;

5 **Figure 9** illustrates how the conductors shown in Figure 7 provide some mechanical support for an integrated circuit component in accordance with one embodiment of the present invention;

Figure 10 illustrates a further embodiment of a transmission line socket configured in accordance with yet another embodiment of the present invention; and

10 **Figure 11** illustrates a cut-away side-view of the transmission line socket in **Figure 10**.

DETAILED DESCRIPTION

Described herein is a socket which includes a first conductor having two or more contact regions and second conductor arranged substantially parallel to the first conductor and also having two or more contact regions. The first and second conductors are spaced relative to one another so as to provide a predetermined electrical impedance. For one embodiment, a dielectric spacer may be disposed between the first and second conductors to provide the spacing. Embodiments of the present invention may find particular use as a socket for accepting integrated circuit (IC) devices, e.g., memory devices such as RDRAMs®, or circuit boards which operate at high frequency. High frequency operation requires careful physical design and a robust electrical interface, both of which are provided by the present invention.

Because the Rambus channel operates at very high frequency with only limited voltage swings between logic levels, any new connector system requires not only a careful physical design but a robust electrical interface. Thus, embodiments of the present invention provide the physical and electrical properties needed to maintain signal integrity on the Rambus channel. At the same time, embodiments of the present invention provide a more manufacturable solution when compared with other means of coupling RDRAMs® to a printed circuit board. Of course, further embodiments of the present invention may also find application wherever a semiconductor device is to be coupled to a substrate (e.g., a motherboard) across a high speed electrical interface.

As shown in Figure 2, a printed circuit board (PC board) 10 may include an application specific integrated circuit (ASIC) or other processing device 12. ASIC 12 may be mounted to PC board 10 using any of number of conventional integrated circuit mounting techniques. For some embodiments, ASIC 12 may be soldered directly to traces on PC board 10. Also mechanically affixed to PC board 10 is a socket 14 configured in accordance with one embodiment of the present invention. Socket 14 may be adapted to accept an RDRAM® or other Daughter card 16. Socket 14, in addition to providing a

mechanical coupling for Daughter card 16, provides a electrical interface between Daughter card 16 and channel 18. Channel 18 includes a number of metal traces laid out on printed circuit board 10 using conventional printed circuit board fabrication techniques and may be configured in accordance with the Rambus Channel physical and/or electrical specifications or other high speed electrical interface requirements.

In general, printed circuit board 10 may include a number of sockets 14. Each socket 14 may be adapted to accommodate two or more Daughter cards 16. Within each socket 14, means of electrically coupling a number of Daughter cards 16 in a substantially bus-like arrangement are provided. In this context, coupling means that there is a separable electrical contact between each Daughter card 16 and the bus. The term bus, as used herein, refers to the interconnect being such that each device (i.e., each Daughter card 16) has an identical (or nearly identical) pinout layout and substantially similar physical dimensions. For example, socket 14 is configured so that each pin "n" of each device contained within socket 14 is connected together. There may be additional electrical connections other than the bus connections, however, the remainder of this description will be directed to the bus-like connections within socket 14.

It is important to recognize that the bus within socket 14 operates at high frequency. That is, the edge rate of the signals present on the electrical connections is comparable to the propagation delay along at least one of the possible signal paths. In general, these connections are referred to as transmission lines.

Proper signaling on transmission lines depends on proper termination, which is commonly performed with resistors. The resistors are selected to have values which match the characteristic impedance of the transmission lines. Therefore, it becomes necessary for the bus to have a known impedance. Accordingly, the electrical conductors which make up the bus-like connection for socket 14 provide a predetermined electrical impedance.

The bus impedance is, in general, determined by the "unloaded" impedance (i.e., the impedance when no Daughter cards 16 are present) as well as the effect of device

loading. In general, all of the relevant pin connections of each of the devices to be inserted in socket 14 have substantially similar loading effects (typically this may be primarily input capacitance). Therefore, the remaining parameter to be controlled is the "unloaded" impedance of the bus connector mechanism. As discussed further below, it is this impedance which is the predetermined impedance provided by the electrical coupling means within socket 14.

Figure 3A illustrates a cross sectional view of printed circuit board 10. Socket 14 is illustrated in dotted outline as is a Daughter card 16. Notice that Daughter card 16 is accommodated in slots within socket 14. The slots provide mechanical coupling and/or support for Daughter card 16 although in other embodiments other mechanical coupling and/or support means may be used. Along printed circuit board 10 is a metal trace 20. Trace 20 forms part of channel 18.

Within socket 14 is a plate 22. Plate 22 is made of metal and is used as a signal conductor for electrical signals transmitted between ASIC 12 and Daughter card 16 along trace 20 of channel 18. As shown, plate 22 includes a number of contact regions 24, contact regions 24 provide an electrical coupling between the associated contact regions where pins of Daughter card 16 and plate 22 touch. In this way, an electrical (i.e., signal) connection is provided from ASIC 12, along trace 20, to plate 22 and contact region 24 to Daughter card 16.

Also provided within socket 14 is an elastomer 26 which is disposed underneath contact region 24. Elastomer 26 provides compliance so that irregularities in plate 22 and/or Daughter card 16 are accounted for. That is, the elastomer 26 provides a springiness so that when Daughter card 16 is inserted in socket 14, contact regions 24 are not broken (e.g., as may occur if the contact regions 24 and/or the plates 22 are fabricated from a relatively stiff material such as a Phosphor-Bronze alloy). In addition, the springiness provided by elastomer 26 helps to support contact regions 24 against corresponding contact regions or pins on Daughter card 16 to maintain a good electrical

connection. In this way, proper electrical coupling is provided. Preferably, elastomer 26 is fabricated from a dielectric material so that proper electrical isolation is maintained if a single elastomer 26 runs through more than one contact region/plate junction.

The multiple contact regions 24 of plate 22 will allow coupling between similar pins of similar Daughter card 16. In this way, the bus-like architecture described above is achieved. A termination network 28 may be provided at the end of the bus for impedance matching.

Plate 22 may be electrically coupled to trace 20 through soldered connections 30 which form electrical contact elements. Other electrical coupling means may also be used.

Plate 22 may have one or more associated posts 32 which may fit into associated holes 34 in PC board 10. In this way, mechanical stability for plate 22 is provided. Plate 22 has only two electrical contact elements (e.g., solder connections 30) to couple to PC board 10 regardless of the number of contact regions 24 disposed along its length. The contact elements may correspond to posts 32 or may be other contact elements.

Preferably, plates such as plate 22 which are signal (and not ground) conductors are electrically coupled to metal traces 20 only at the ends of plate 22. This is important so that only plate 22 acts as a signal carrying bus through socket 14. The reason for isolating the signal carrying buses from the PC board 10 in this fashion is to ensure that the impedance of the signal carrying bus with respect to the ground busses is determinable. If the signal carrying busses were soldered to the printed circuit board at various points throughout the length of the bus (e.g., plate 22) there would be no guarantee that all the solder connections were made or that the connections were fabricated in the same fashion and so the impedance of the signal bus could not be determined with high accuracy.

In contrast, where plates 22 are used as ground (and not signal) conductors, the plates 22 are preferably "stitched" or redundantly connected (e.g., by solder connections) to the ground system of the printed circuit board 10 by means of electrical contacts at variety of intervals along the length of the plate 22. For example, for a plate 22 which is

used as a ground bus bar, the plate may have a number of metal posts 32 at regularly spaced intervals along its length, each being soldered to a ground trace or other reference plane on PC board 10. Thus, the signal bus bars and the ground bus bars (each of which may be fabricated as metal plates 22) are physical opposites in that the signal bus bars are isolated from the printed circuit board 10 over their signal carrying lengths while the ground bus bars are intimately connected to the printed circuit board 10 reference plane over their lengths.

Figure 3B illustrates the ground contact design described above. A plate 22 which is adapted to carry an electrical ground within socket 14 (shown in dotted outline) has electrical contact elements, e.g., solder connections 30, at either end and also has several posts 32 which act as further electrical contact elements coupled to a ground plane 35 at corresponding thru-hole connections 37 along the length of plate 22. The thru-hole connections 37 provide additional protection against excessive ground bounce and further provide mechanical stability for plate 22. Note that the number of electrical connections between plate 22 and ground plane 35 depends only on the number of electrical contact elements, such as solder connections 30 and thru-hole connections 37, and not on the number of contact regions 24 disposed along the length of plate 22. Notice also that, for this embodiment, contact regions 24 provide mechanical support for Daughter cards 16 in place of (or in addition to) slots in socket 14.

A number of plates 22, disposed substantially parallel to one another, will be provided within socket 14 to connect like pins of various Daughter cards 16. The spacing of plates 22 is controlled so as to provide the required unloaded electrical impedance to ensure proper operation at high frequency. Figure 4 illustrates in more detail one means of providing the proper spacing and electrical coupling between plates. As shown, a first plate 22a and second plate 22b may be separated by a dielectric spacer 36. Each of the plates 22a and 22b may be bonded to the dielectric spacer 36 and pressed together so as to achieve the desired spacing between elements. Elastomer 26 is provided between contact

regions 24 and the remainder of the plate 26 to provide compliance as described above. In other embodiments, the electrical properties provided by dielectric spacer 36 may be achieved by using an air gap between plates 22a and 22b.

In order to provide proper signal integrity, channel 18 and, hence, plates 22 within socket 14, is/are organized so that cross-talk between signal lines is reduced or eliminated. This may be achieved, in one embodiment, as illustrated in Figure 5. As shown, the traces 20 on printed circuit board 10 which make up channel 18 are arranged in pairs of signal lines (S) and ground (AC) lines (G). That is, the traces 20 are arranged as signal, signal; ground, ground; signal, signal, etc. and are spaced at a desired distance "d" to achieve desired electrical characteristics (e.g., a desired impedance). The conductors within socket 14 carry the respective signals or grounds from channel 18.

Figure 6A illustrates an alternative embodiment for the electrical conductors within socket 14. In this case, plates 22 have been replaced with conductors 40. Conductors 40 include contact regions 42 which are formed as taps or fingers. In general, conductors 40 may be stamped from metal and may lie flat along the bottom of socket 14. Appropriate electrical connection between traces 20 and conductors 40 is provided (e.g., using a solder connection). As shown in Figure 6B, contact regions 42 are bent so as to form contact pads 46. Contact pads 46 may then provide electrical coupling between corresponding contact regions or pins on Daughter card 16 and conductor 40.

Figure 7 illustrates in more detail a Daughter card 16. As shown, Daughter card 16 comprises an integrated circuit (IC) component 50, for example a DRAM chip, and a plurality of leads 52. Leads 52 extend from IC component 50 in a fan out pattern to one edge of Daughter card 16. The leads 52 may be metal traces on a suitable flexible material overlaid over a rigid support member, e.g., a metal plate. In general, leads 52 may be present on both sides of Daughter card 16 and may terminate in larger contact pads or pins.

For the situation where leads are present on both sides of Daughter card 16, an alternative electrical connection within socket 14 may be provided using conductors 60a

and 60b as illustrated in Figure 8. Conductors 60a and 60b may be formed as metal plates as for the embodiment illustrated in Figure 3 or as essentially flat conductors as for the embodiment shown in Figure 6A. Contact regions 62a and 62b are formed using tabs or fingers similar to the embodiment illustrated in Figures 6A and 6B. As shown, conductor 5 60a may be used for a ground signal and conductor 60b may be used as a signal carrying conductor, for example, where traces 20 (not shown) are arranged as signal, signal; ground, ground; etc. as discussed above.

In one embodiment, conductors 60a and 60b may be disposed within socket 14 so that contact region 62a makes contact with a pin or lead on one side of Daughter card 16 10 while conductor 62b makes contact with a pin or lead (or other contact region) on the opposite side of Daughter card 16. This arrangement is illustrated in Figure 9. Such an arrangement provides additional mechanical support for Daughter card 16 within socket 14.

Figure 10 illustrates a top view of a further embodiment of a transmission line socket 70 in accordance with yet another embodiment of the present invention. Socket 70 15 is illustrated as a four-site socket with three signal lines 72, however, this is for purposes of example only and the present invention is applicable to a single or multiple-site socket having a plurality of signal lines. Plug-in devices (e.g., Daughter cards 16) may be accepted within any of the slots 74 and the electrical conductors 72 and 76 are arranged so that the plug-in devices are contacted by the conductors on both the front and back sides, 20 thereby reducing the effective signal spacing on the plug-in device and easing associated mechanical tolerance requirements. Electrical conductors 72 and 76 are configured as bus bar transmission lines with solder connections at either end of socket 70.

In this embodiment, the electrical signals within socket 70 are ordered as signal, ground, signal, etc. Such a distribution aids in achieving uniform impedance and minimal 25 crosstalk, however, it is necessary that this same signal distribution pattern be maintained not only between the conductors 72 and 76, but also between contact areas on the plug-in devices. If the electrical contact areas of the conductors 72 and 76 were arranged so as to

alternate connections between the front and back sides of a plug-in device, all the signal connections (from conductors 72) would end up on one side of the plug-in device while all the ground connections (from conductors 76) would end up on the other side. This would yield poor electrical qualities because the inductive loop area would be increased, resulting in greater contact inductance.

This problem is solved in this embodiment by forming the contact regions of the conductors 72 and 76 so that each row of contacts is bent such that the point where the contact touches the plug-in device is off-set by one-half of the pitch (i.e., the distance between contact regions or pins on the plug-in device). That is, each pair of adjacent signal and ground conductors, 72 and 76, have respective contact regions bent towards one another in a vertical plane. The result is illustrated in Figure 11 which depicts a cut-away side-view of socket 70. The effect of this forming pattern is that both sides of the plug-in device will contact in a signal, ground, signal, etc. pattern, which maintains good signal isolation and inductance characteristics. The impedance of the transmission line socket 70 may be selected by varying the width, thickness and spacing of the conductors 72 and 76, as well as the ratio of socket body material to air gap spacing separating the conductors.

To provide compliance, contact regions 62a and 62b (and conductors 60a and 60b, if desired) of Figure 8 and/or conductors 72 and 76 of Figure 10 may be made from a springy metal such as a Beryllium-Copper (Be-Cu) alloy or another metal. Alternatively, the contact regions may be elastomer-backed metal regions as discussed with reference to Figure 3. In such a case, the elastomer may be supported by a wall or other region of socket 14. In other embodiments, socket 14 may be a plug (i.e., a non-compliant component of the coupling system) and a compliant coupling region may be provided on Daughter card 14.

Embodiments of the present invention avoid the one-to-one correspondence between the number of contact regions and contact elements which were found in connectors of the past. The one-to-one correspondence of contact regions to contact

elements which characterized previous connectors lead to a very high density of contact elements to the substrate (i.e., the printed circuit board). This, in turn, lead to a device which was not readily manufacturable because there was no way to guarantee good connections between the contact elements and the substrate. By avoiding the one-to-one correspondence between contact elements and contact regions, these embodiments of the present invention reduce the density of the connections to the substrate, thereby achieving a more manufacturable device.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. For example, although RDRAMs® have been referred to in this application, other types of devices are contemplated, including other DRAMs, integrated circuits, memories, circuit boards, and other components requiring an electrical connection to a substrate. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

- 1 1. A socket, comprising:
2 a first conductor having two or more contact regions; and
3 a second conductor arranged substantially parallel to said first conductor and having
4 two or more contact region,
5 wherein said first and second conductors are spaced relative to one another so as to
6 provide a predetermined electrical impedance.
- 1 2. A socket as in claim 1 further comprising a dielectric spacer disposed between said first
2 and second conductors.
- 1 3. A socket as in claim 2 wherein said contact regions of said first and second conductors
2 provide compliant coupling regions for said socket.
- 1 4. A socket as in claim 3 wherein said contact regions of said first and second conductors
2 are made of a Beryllium-Copper (Be-Cu) alloy.
- 1 5. A socket as in claim 3 wherein said contact regions of said first and second conductors
2 comprise an elastomer-backed metal region.
- 1 6. A socket as in claim 2 wherein said contact regions of said first and second conductors
2 comprise fingers offset from said respective conductors through a bend.
- 1 7. A socket as in claim 1 wherein said contact regions of said first and second conductors
2 comprise compliant coupling regions.
- 1 8. A socket as in claim 1 wherein said contact regions comprise non-compliant coupling
2 regions.

08697706, 0702197

1 9. A socket as in claim 1 wherein said contact regions of said first conductor are arranged
2 to contact a lead disposed on a first side of a circuit element and said contact regions of said
3 second conductor are arranged to contact a lead disposed on a second side of said circuit
4 element.

1 10. A socket as in claim 1 wherein said first conductor is further adapted to be coupled to a
2 substrate through only two electrical contact elements over its length, regardless of the
3 number of contact regions of said first conductor.

1 11. A socket as in claim 10 wherein said second conductor is further adapted to be coupled
2 to said substrate through a number of electrical contact elements disposed along its length,
3 the number of contact elements being independent of the number of contact regions of said
4 second conductor.

1 12. An electrical connector, comprising:
2 a socket; and
3 a plurality of conductors disposed within said socket and arranged to carry electrical
4 signals as transmission lines, said conductors being arranged into a first group of
5 conductors each adapted to be coupled to a substrate at only two electrical contact elements
6 and a second group of conductors each adapted to be coupled to said substrate at a plurality
7 of electrical contact elements.

1 13. A connector as in claim 12 wherein said conductors each include compliant contact
2 regions.

1 14. A connector as in claim 13 wherein said contact regions of said conductors are
2 arranged such that the contact regions of a first of said conductors are positioned within
3 said socket so as to contact a lead disposed on a first side of a circuit element and the

4 contact regions of a second of said second conductors are positioned within said socket so
5 as to contact a lead disposed on a second side of said circuit element.

1 15. A connector as in claim 14 further comprising a dielectric spacer disposed between
2 said first and second conductors.

1 16. A connector as in claim 13 wherein said contact regions of said conductors are made of
2 a Beryllium-Copper (Be-Cu) alloy.

1 17. A connector as in claim 13 wherein said contact regions of said conductors comprise
2 elastomer-backed metal regions.

1 18. A connector as in claim 14 wherein said contact regions of said first and second
2 conductors comprise fingers offset from said respective conductors through a bend.

1 19. A circuit board, comprising:

2 a compliant electrical connector having a plurality of conductors arranged into a first
3 group of conductors each adapted to be coupled to a substrate at only two electrical contact
4 elements and a second group of conductors each adapted to be coupled to said substrate at a
5 plurality of electrical contact elements; and

6 an electrical channel coupled to said connector.

1 20. A circuit board as in claim 19 wherein said electrical channel comprises a plurality of
2 traces.

1 21. A circuit board as in claim 20 wherein each of said plurality of electrical conductors
2 further includes two or more contact regions, the number of contact regions of each
3 conductor being independent of the number of electrical contact elements of a respective
4 conductor.

1 22. A circuit board as in claim 21 wherein said contact regions of said conductors
2 comprise fingers offset from said conductors through a bend.

1 23. A circuit board as in claim 21 wherein said contact regions of said conductors
2 comprise elastomer-backed metal regions.

1 24. A connector, comprising:

2 a first electrical signal path configured to provide a bus-like interconnection between
3 similar electrical couplings of two or more electrical components, said bus-like
4 interconnection adapted to be isolated from a circuit board except for two electrical contact
5 elements disposed near opposite ends of said first electrical signal path; and
6 a ground signal path.

1 25. A connector as in claim 24 wherein said ground signal path is configured as a second
2 electrical signal path arranged to provide a bus-like interconnection between similar
3 electrical couplings of said two or more electrical components.

1 26. A connector as in claim 25 wherein said ground signal path is adapted to be electrically
2 coupled to a ground plane of said circuit board at a plurality of points along said bus-like
3 interconnection.

1 27. A connector as in claim 26 wherein said first electrical signal path comprises an
2 electrical conductor having compliant contact regions.

1 28. A connector as in claim 27 wherein said compliant contact regions comprise elastomer-
2 backed metal regions.

1 29. A connector as in claim 27 wherein said compliant contact regions are made of a
2 Beryllium-Copper (Be-Cu) alloy.

30. A socket, comprising:

a conductive signal bar including two or more contact regions, each adapted to couple to a contact region on a respective electrical device, said signal bar further adapted to be electrically coupled to a circuit board through only two electrical contact elements regardless of the number of contact regions of said signal bar; and

a conductive ground bar arranged substantially parallel to said signal bar, said ground bar having two or more contact regions, each adapted to couple to a contact region on said respective electrical devices, and further being adapted to be electrically coupled to a conductive reference region of said circuit board at a number of electrical contact elements, the number of electrical contact elements being independent of the number of contact regions of said ground bar.

31. A socket as in claim 30 wherein said electrical contact elements of said conductive signal bar comprise metal posts disposed near the ends of said conductive signal bar.

32. A socket as in claim 31 wherein said electrical contact elements of said ground bar comprise metal posts disposed so as to electrically couple said ground bar to said reference region at a plurality of positions throughout the length of said ground bar.

33. A socket as in claim 32 wherein said posts of said ground bar are disposed at approximately equal intervals over the length of said ground bar.

34. A socket as in claim 30 further comprising a plurality of said conductive signal bars and conductive ground bars arranged to alternate in a signal, ground, signal, ground, etc. pattern.

35. A socket as in claim 30 wherein said ground bar is arranged substantially parallel to said signal bar such that the transmission line impedance between said ground bar and said signal bar is determinable.

ABSTRACT

A socket includes a first conductor having two or more contact regions and a second conductor arranged substantially parallel to the first conductor and having two or more contact regions. The first and second conductors are spaced relative to one another so as to provide a predetermined electrical impedance and may be arranged to carry electrical signals as transmission lines. A dielectric spacer may be disposed between the first and second conductors to provide the spacing. Contact regions of the first and second conductors may provide compliant coupling regions for the socket. The contact regions of the first conductor may be positioned within the socket so as to contact a lead disposed on a first side of a circuit element and the contact regions of the second conductor may be positioned within the socket so as to contact a lead disposed on a second side of the circuit element. The first conductor may be further adapted to be coupled to a substrate through only two electrical contact elements over its length, regardless of the number of contact regions of the first conductor. In addition, the second conductor may be further adapted to be coupled to the substrate through a number of electrical contact elements disposed along its length, the number of contact elements being independent of the number of contact regions of the second conductor.

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"MULTI-POSITION CONNECTOR WITH INTEGRAL TRANSMISSION LINE BUS"

the specification of which

X is attached hereto.
_____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority
Claimed

(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Berezna, Reg. No. 33,474; Michael A. Bernadico, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; William Donald Davis, Reg. No. 38,428; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Karen L. Feisthamel, Reg. No. 40,264; James Y. Go, Reg. No. P-40,621; Tarek N. Fahmi, Reg. No. P-41,402; David R. Halvorson, Reg. No. 33,395; Eric Ho, Reg. No. 39,711; George W. Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; Stephen L. King, Reg. No. 19,180; Dolly M. Lee, Reg. No. 39,742; Michael J. Mallie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Robert Andrew Diehl, Reg. No. P-40,992; Sharmini Nathan Green, Reg. No. P-41,410; Thomas A. Hassing, Reg. No. 36,159; Edwin A. Sloane, Reg. No. 34,728; and Judith A. Szepesi, Reg. No. 39,393; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Tarek N. Fahmi, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and
direct telephone calls to Tarek N. Fahmi, (408) 720-8598.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Donald Victor Perino

Inventor's Signature _____ Date _____

Residence Los Altos, CA Citizenship U.S.
(City, State) (Country)

Post Office Address 1690 William Henry Court
Los Altos, CA 94024

Full Name of Second/Joint Inventor John Bradly Dillon

Inventor's Signature _____ Date _____

Residence Palo Alto, CA Citizenship U.S.
(City, State) (Country)

Post Office Address 177 Monroe Drive
Palo Alto, CA 94306

Full Name of Third/Joint Inventor James Anthony Gasbarro

Inventor's Signature _____ Date _____

Residence Mountain View, CA Citizenship U.S.
(City, State) (Country)

Post Office Address 1613 Notre Dame Drive
Mountain View, CA 94040

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
 - (2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.
- (b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and
- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
 - (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

- (c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:
- (1) Each inventor named in the application;
 - (2) Each attorney or agent who prepares or prosecutes the application; and
 - (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.
- (d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

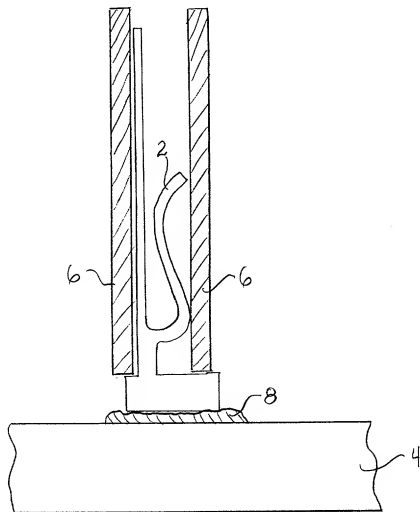


Fig. 1 (Prior Art)

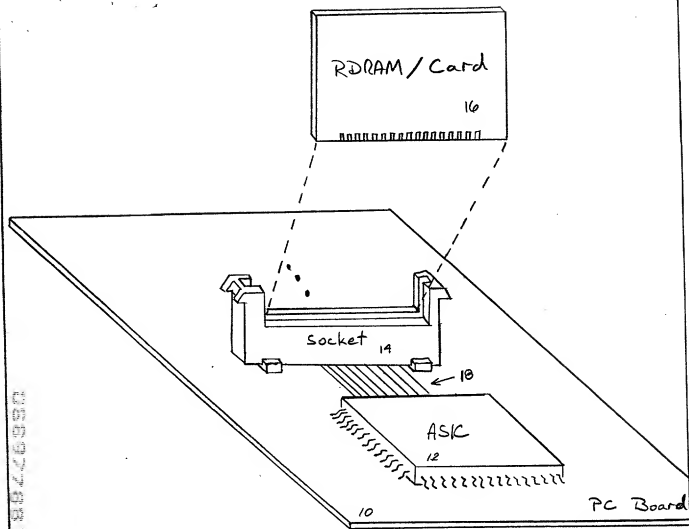


Fig. 2



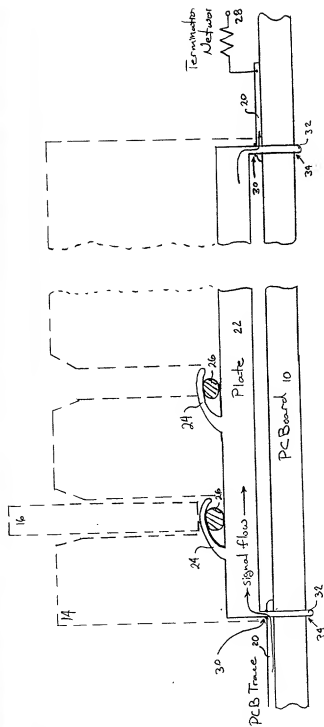


Fig. 3A



267270 88/6880

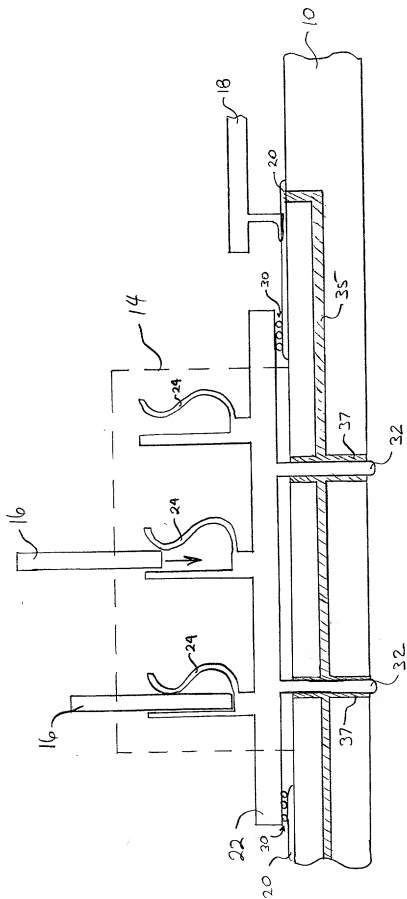


Fig. 3B

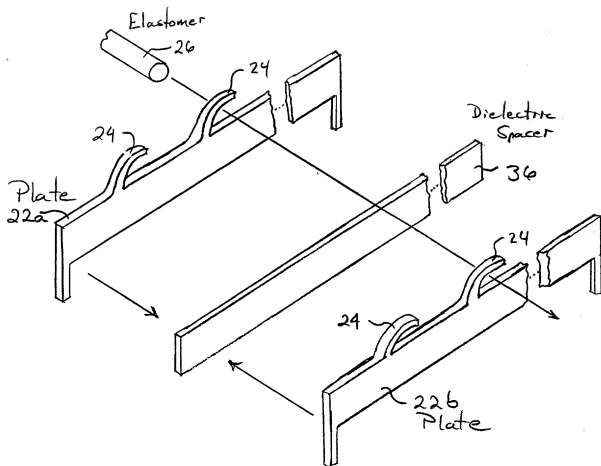


Fig. 4



22-141 50 SHEETS
 22-142 100 SHEETS
 22-144 200 SHEETS

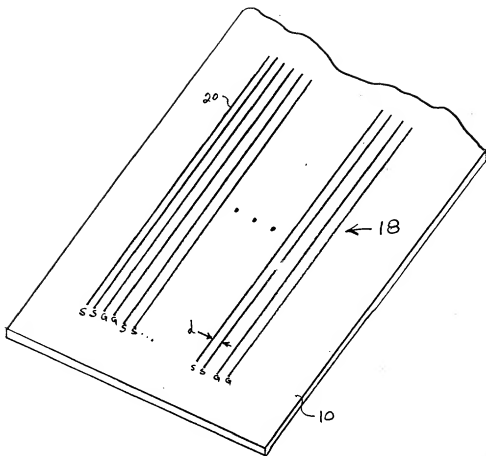
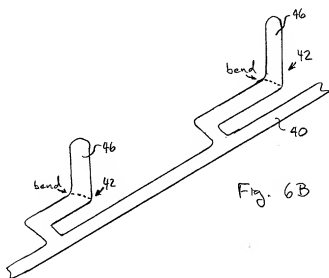
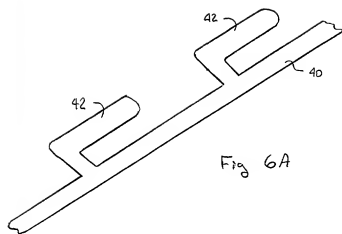


Fig. 5

10889788-07497
757270-9876883



50 SHEETS
22-141
100 SHEETS
22-142
200 SHEETS
22-144



467270-8876890

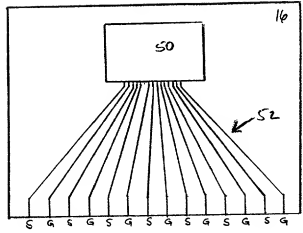


Fig. 7



251275-88/6980

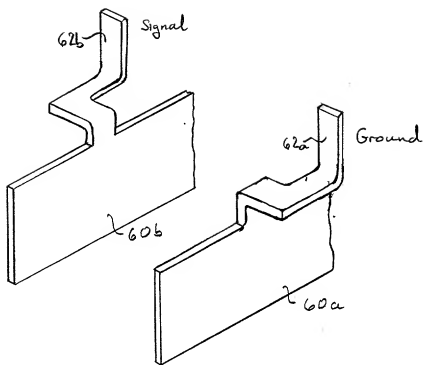


Fig. 8

22-141 40 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS

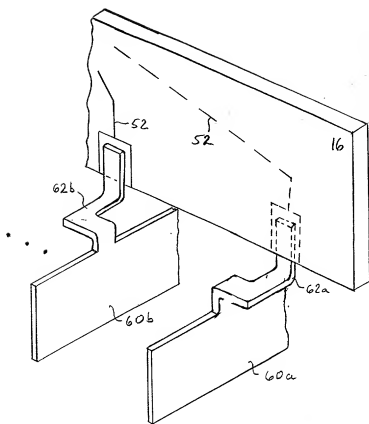


Fig. 9

08897788-072197

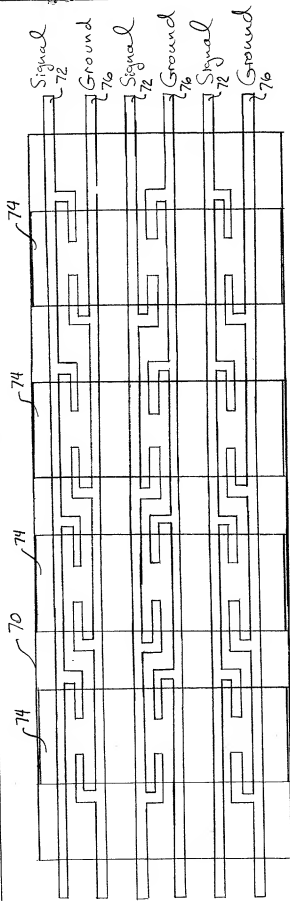


Fig. 10

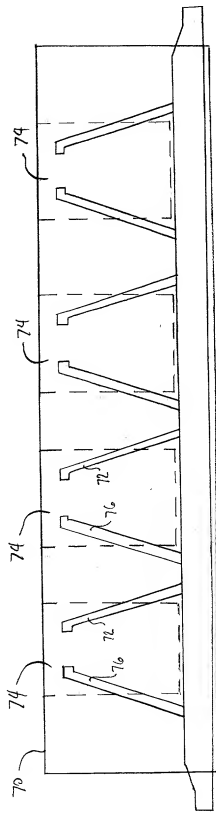


Fig. 11